Subtractors:

Half-Subtractor: The half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, the minuend **X** and subtrahend **Y** and two outputs the difference **D** and $\mathbf{B_{out}}$.

The truth table for the half-Subtractor is as shown below.

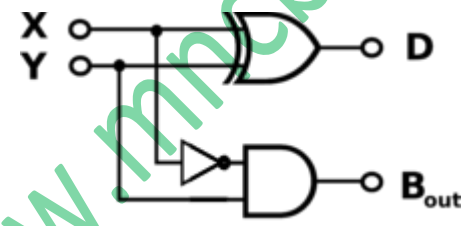
Inputs		Outputs	
X	*Y*	*D*	B_{out}
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Using the table above and a K-Map, we find the following logic equations for **D** and $\mathbf{B_{out}}$.

$\mathbf{D} = X \oplus Y$

$\mathbf{B_{out}} = X'.Y$

The logic diagram of a half-subtractor is as shown below.



Full Subtractor: The full subtractor is a combinational circuit which is used to perform subtraction of three input bits: the minuend **X**, subtrahend **Y**, and Borrow in ($\mathbf{B_{in}}$). The full subtractor generates two output bits: the difference **D** and Borrow out ($\mathbf{B_{out}}$)

The truth table for the Full-Subtractor is given below:

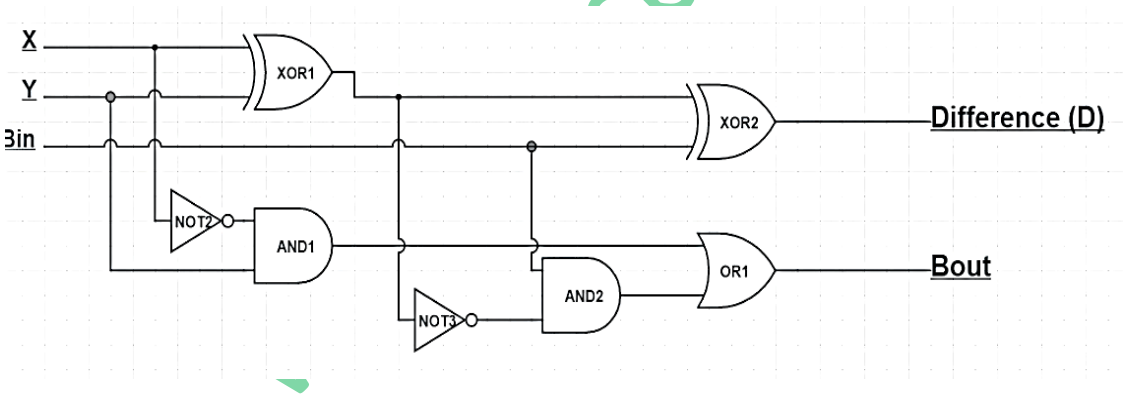
Inputs			Outputs	
X	***Y***	B_{in}	***D***	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Therefore the equations for **D** and $\mathbf{B_{out}}$ after simplification are:

$$\mathbf{D = X \oplus Y \oplus B_{in}}$$

$$\mathbf{B_{out} = X'B_{in} + X'Y + YB_{in}}$$

The circuit diagram of a Full-Subtractor is shown below



Encoder: An encoder is a combinational circuit that converts binary information in the form of a 2N input lines into N output lines, which represent N bit code for the input. For simple encoders, it is assumed that only one input line is active at a time.

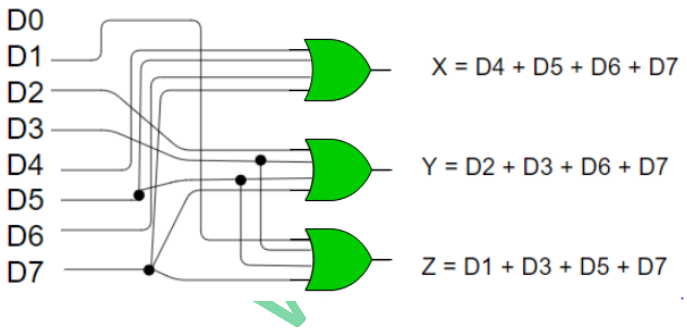
'ruth Table –

D7	D6	D5	D4	D3	D2	D1	D0	X	Y	Z
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

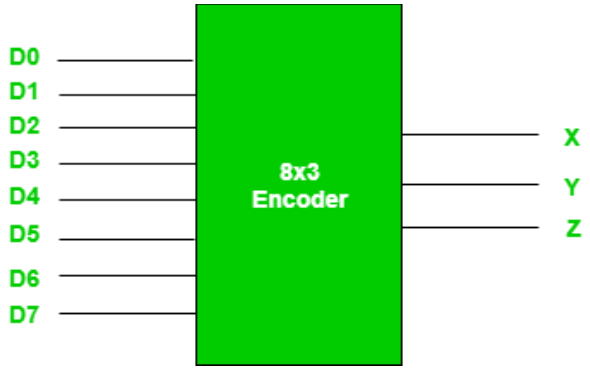
As seen from the truth table, the output is 000 when D0 is active; 001 when D1 is active; 010 when D2 is active and so on. The output equations are

X = D4 + D5 + D6 + D7
Y = D2 +D3 + D6 + D7
Z = D1 + D3 + D5 + D7

The circuit diagram can be drawn as below



Example: Let us consider **Octal to Binary** encoder. As shown in the following figure, an octal-to-binary encoder takes 8 input lines and generates 3 output lines.



Decoder: A decoder does the opposite job of an encoder. It is a combinational circuit that converts n lines of input into 2^n lines of output. The truth table of 3-to-8 line decoder is shown below.

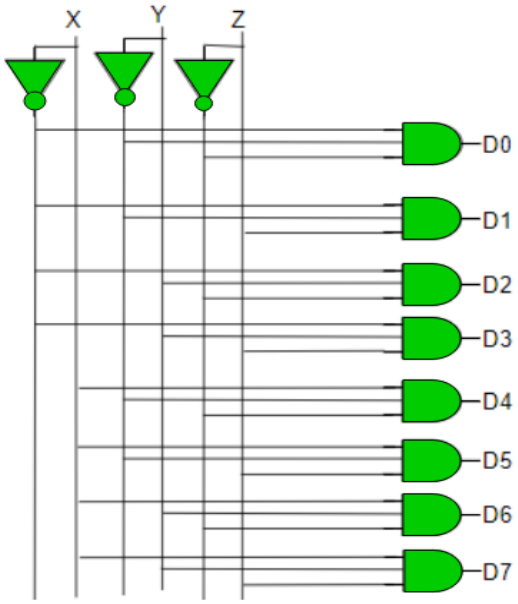
Here, x, y, z are three input lines and D0 to D7 are eight output lines.

X	Y	Z	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Output equations are:

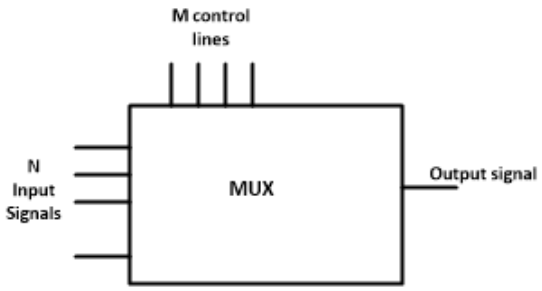
$D0 = x'y'z'$ $D1 = x'y'z$ $D2 = x'yz'$ $D3 = x'yz$
$D4 = xy'z'$ $D5 = xy'z$ $D6 = xyz'$ $D7 = xyz$

Circuit diagram is given below



Multiplexer (MUX): Multiplexer means many into one. A multiplexer is a circuit used to select and route any one of the several input signals to a signal output. Multiplexer handle two type of data that is analog and digital. For analog application, multiplexer are built of relays and transistor switches. For digital application, they are built from standard logic gates.

Following figure shows the general idea of a multiplexer with n input signal, m control signals and one output signal.



Example: 4x1 Multiplexer

The 4-to-1 multiplexer has 4 input bit, 2 control bits, and 1 output bit. Here, the four input bits are D0, D1, D2 and D3. Only one of this is transmitted to the output y at a time. The output depends on the value of S_0 and S_1 which is the control input. The control input determines which of the input data bit is transmitted to the output. The truth table is given below.

Select Data Inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

The circuit diagram is shown below. It works according to the truth table. When S_0S_1 = 00, the upper AND gate is enabled while all other AND gates are disabled. Therefore, data bit D_0 is transmitted to the output, giving Y = D_0. Similarly, when S_0S_1=11, all gates are disabled except the bottom AND gate. In this case, D_3 is transmitted to the output and Y = D_3.

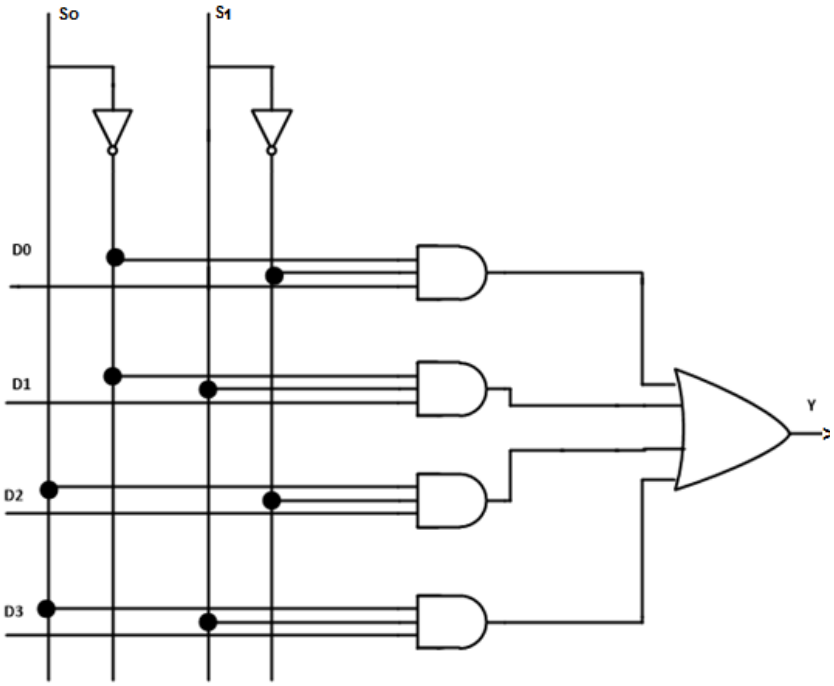
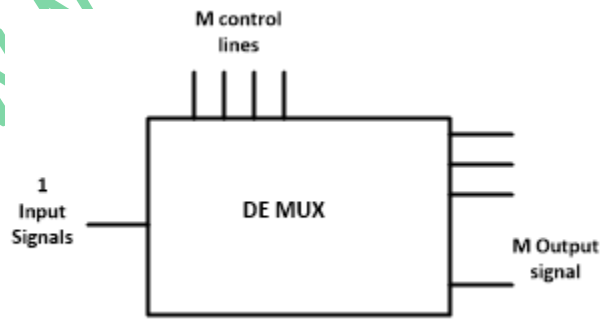


Fig: 4 to 1 Multiplexer Circuit Diagram

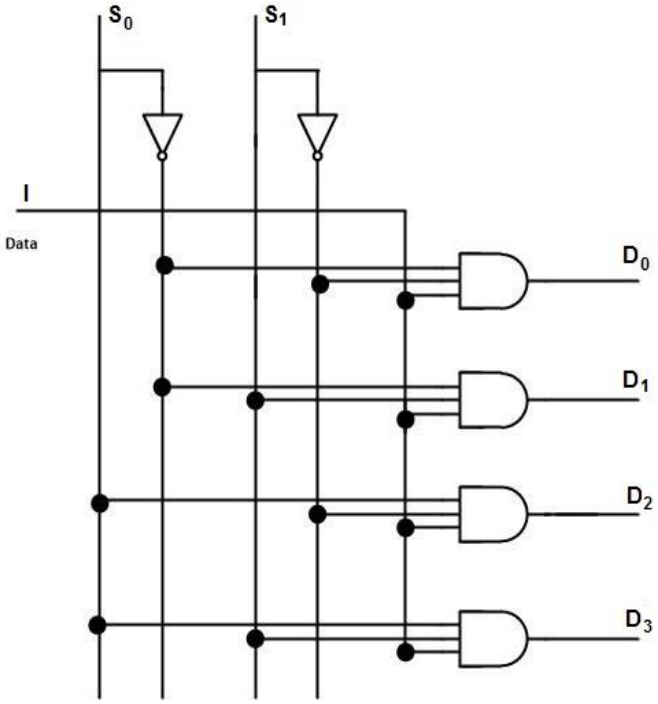
De-multiplexer (DMUX): De-multiplexer means one to many. A De-multiplexer is a circuit with one input and many outputs. Following figure illustrates the general idea of a de-multiplexer with 1 input signal, m control signals, and n output signals.



Example: 1x4 DMUX

The 1-to-4 demultiplexer has 1 input bit, 2 control bit, and 4 output bits. In the following example, I is the input line, S_0 and S_1 are two control lines, D_0, D_1, D_2, D_3 are four output lines. The truth table and circuit diagram of a 1-to-4 DMUX is shown in below.

Input	Select Lines	Output Lines
I	S_1 S_0	D_0 D_1 D_2 D_3
I	0 0	1 0 0 0
I	0 1	0 1 0 0
I	1 0	0 0 1 0
I	1 1	0 0 0 1



The input data bit **(I)** is transmitted to the data bit of the output lines **(D)**. This depends on the value of S_0 and S_1, the control input.

When AB = 00, the upper **First** AND gate is enabled while other AND gates are disabled. Therefore, only data bit D is transmitted to the output, giving $D_0 = I$.

Similarly, when control input is changed to AB = 11, all the gates are disabled except the **Fourth** AND gate from the top. Then, **I** is transmitted only to the D_3 output.